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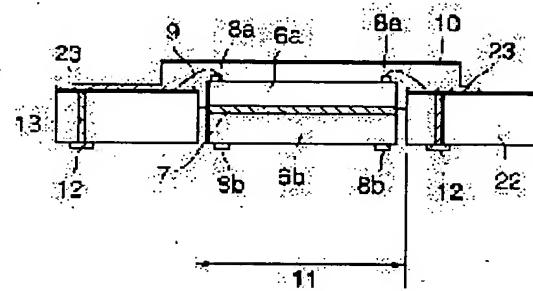
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## (54) SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

## (57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device having an MCP structure, in which a plurality of semiconductor elements are laminated, with a plurality of semiconductor elements having substantially the same shape, and to provide a method of manufacturing the same.

SOLUTION: This semiconductor device includes a wiring board 22, having a front surface and a rear surface, an interconnect line 23 formed at least on the front surface, an opening 11 formed in the wiring board 22 reaching the rear surface from the front surface, a first surface, on which a first electrode 8a is formed, and a second surface opposed to the first electrode 8a. This semiconductor device is constituted by a first semiconductor element 6a, having the second surface disposed in the opening 11, a metal filament 9, which is a first conductor for connecting the first electrode 8a and the interconnect line 23, a sealing body 10 for sealing the first semiconductor element 6a and the metal filament 9 and fixing the first semiconductor element 6a to the wiring board 22, and a second semiconductor element 6b, which is fixed on the second surface, has a third surface fixed to the second surface and a forth surface opposed to the third surface, has a second electrode 8b for external connection formed on the fourth surface and has substantially the same shape as that of the first semiconductor element 6a.



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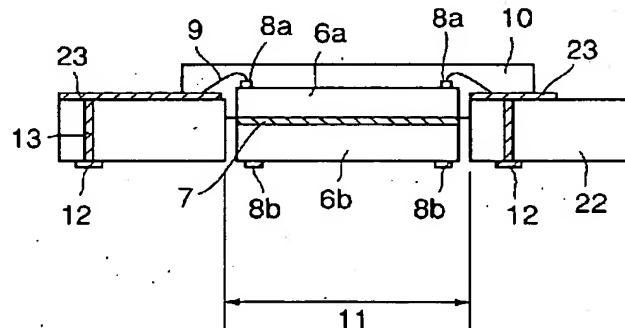
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(54)【発明の名称】 半導体装置及びその製造方法

(57)【要約】

【目的】 複数の半導体素子が積層されたMCP構造を有する半導体装置において、略同一形状を有する複数の半導体素子が実装されたMCP構造の半導体装置、及びその製造方法を提供することを目的とする。

【構成】 半導体装置は、表面及び裏面を有する配線基板22と、少なくとも表面に形成される配線23と、配線基板22に形成され、表面から裏面に至る開口部11と、第1の電極8aが形成された第1の面と、その第1の面に対向する第2の面とを有し、開口部11内に配置される第2の面を有する第1の半導体素子6aと、第1の電極8aと配線23とを接続する第1の導体である金属細線9と、第1の半導体素子6aと金属細線9とを封止するとともに、第1の半導体素子6aを配線基板22に固定する封止体10と、第2の面上に固定されるとともに、第2の面と固定される第3の面、及び第3の面に対向する第4の面を有し、第4の面には、外部との接続を行なう第2の電極8bが形成され、かつ、第1の半導体素子6aと略同一形状を有する第2の半導体素子6bとから構成される。



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## 【特許請求の範囲】

【請求項 1】 第1の面を有する第1の基板、及び前記第1の面上に配置される第2の基板とからなる配線基板と、前記第1の面より前記第1の基板に形成される凹部と、前記凹部に対応する前記第2の基板に設けられ、前記凹部に対応する領域よりも広い領域に形成される開口部と、前記凹部内に配置されるとともに、前記配線基板に形成された配線パターンに電気的に接続される第1の電極を有する第1の半導体素子と、

一部分が前記開口部内の前記第1の面上に配置される第2の半導体素子とを有することを特徴とする半導体装置。

【請求項 2】 前記第2の半導体素子は、前記第1の半導体素子と略同一形状を有することを特徴とする請求項1記載の半導体装置。

【請求項 3】 前記配線基板は、前記第1の基板及び前記第2の基板とが一体的に形成されることを特徴とする請求項1記載の半導体装置。

【請求項 4】 請求項1記載の半導体装置は、更に、前記第1の電極と前記配線基板とを電気的に接続する金属細線を有しており、

前記第1の電極は、前記第2の半導体素子により規定される領域以外の前記第1の半導体素子の領域に設けられていることを特徴とする半導体装置。

【請求項 5】 表面及び裏面を有する配線基板と、少なくとも前記表面に形成される配線と、

前記配線基板に形成され、前記表面から前記裏面に至る開口部と、

第1の電極が形成された第1の面と前記第1の面に対応するとともに、前記開口部内に配置される前記第2の面を有する第1の半導体素子と、

前記第1の電極と前記配線とを接続する第1の導体と、前記第1の半導体素子と前記第1の導体とを封止するとともに、前記第1の半導体素子を前記配線基板に固着する封止体と、

前記第2の面上に固定されるとともに、前記第2の面と固定される第3の面、及び前記第3の面に対応する第4の面を有し、前記第4の面には、外部との接続を行なう第2の電極が形成され、かつ、前記第1の半導体素子と略同一形状を有する第2の半導体素子とを有することを特徴とする半導体装置。

【請求項 6】 前記裏面と前記第4の面とは、略同一面を形成していることを特徴とする請求項5記載の半導体装置。

【請求項 7】 表面及び裏面を有する配線基板の第1領域に、前記表面から前記裏面に至る開口部を形成する工程と、

前記第1領域よりも小さい面積を有する上面と、前記表面及び前記裏面間の距離により規定される高さよりも低い高さとからなる凸部を有する実装部材を準備する工程

と、

前記裏面より前記実装部材の前記凸部を挿入する工程と、

第1の電極が形成される第1の面と、前記第1の面に対応する第2の面とを有する第1の半導体素子を前記開口部内の前記凸部上に固定する工程と、

前記第1の半導体素子を固定する工程後、前記第1の電極と前記表面上の配線とを第1の導体で接続する工程と、前記第1の半導体素子及び前記第1の導体を封止体で封止

するとともに、前記封止体により前記第1の半導体素子を前記配線基板に固着する工程と、前記固着する工程後、前記実装部材を除去する工程と、前記除去する工程後、第2の電極が形成される第3の面と前記第3の面に対応する第4の面を有するとともに、前記第1の半導体素子と略同一形状を有する第2の半導体素子の前記第4の面を前記第2の面上に固定する工程とを有することを特徴とする半導体装置の製造方法。

【請求項 8】 前記凸部上には、粘着性を有する物質が設けられていることを特徴とする請求項7記載の半導体装置の製造方法。

【請求項 9】 前記実装部材は、前記凸部と前記凸部を搭載するシートから構成されており、前記シートは粘着性を有していることを特徴とする請求項7記載の半導体装置の製造方法。

【請求項 10】 請求項7記載の半導体装置の製造方法において、

前記第2の電極は、外部との接続を行なう電極であることを特徴とする半導体装置の製造方法。

【請求項 11】 請求項10記載の半導体装置の製造方法において、

前記第2の半導体素子を固定する工程は、前記裏面と前記第3の面とが略同一平面を形成するように行われるこことを特徴とする半導体装置の製造方法。

【請求項 12】 請求項7記載の半導体装置の製造方法において、更に、

前記第2の半導体素子を固定する工程後、前記第2の電極と前記裏面上の配線とを第2の導体で接続する工程と、

前記第2の半導体素子及び前記第2の導体を封止体で封止するとともに、前記第2の半導体素子及び前記第2の導体を封止する封止体により前記第2の半導体素子を前記配線基板に固着する工程とを有することを特徴とする半導体装置の製造方法。

【請求項 13】 第1の面を有する絶縁基板と、前記第1の面に形成される第1の溝と、前記第1の溝の底面に形成され、前記底面の面積よりも小さい面積を有する第2の溝と、前記第2の溝内に配置されるとともに、前記絶縁基板に形成された配線パターンに電気的に接続される第1の電極を有する第1の半導体素子と、

一部分が前記第2の溝内にある前記第1の面上に配置される第2の半導体素子とを有することを特徴とする半導体装置。

【請求項14】 前記第2の半導体素子は、前記第1の半導体素子と略同一形状を有することを特徴とする請求項13記載の半導体装置。

【請求項15】 請求項13記載の半導体装置は、更に、前記第1の電極と前記配線基板とを電気的に接続する金属細線を有しており、

前記第1の電極は、前記第2の半導体素子により規定される領域以外の前記第1の半導体素子の領域に設けられていることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は、半導体装置及びその製造方法に関し、特に薄型化、高密度実装可能な半導体装置及びその製造方法に関するものである。

【0002】

【従来の技術】 従来、高密度実装可能な半導体装置を実現するため、1つのパッケージ内に複数の半導体装置を実装するMCP (Multi-Chip-Package) 構造を採用している。

【0003】 通常のMCP構造を有する半導体装置では、回路配線が形成された配線基板上に、表面に電極を有する第1の半導体素子が実装される。更に、その第1の半導体素子の電極を除く表面上には、絶縁性を有する接着材が設けられ、その接着材によって第2の半導体素子が積層される。

【0004】 また、従来の半導体装置では、第2の半導体素子が第1の半導体素子上に積層された後、各半導体素子に形成された電極と配線基板に形成された回路配線とが金属細線により接続され、各半導体素子と配線基板とが電気的に接続されている。さらに、各半導体素子と金属細線は樹脂からなる封止体により封止され、保護される。

【0005】

【発明が解決しようとする課題】 しかしながら、上記に述べた従来のMCP構造を有する半導体装置では、電極が形成されている第1の半導体素子の面上に、第2の半導体素子が直接配置されており、第1の半導体素子上に形成された電極と配線基板上の回路配線とを金属細線により接続することで、第1の半導体素子と配線基板との電気的接続を行なっている。

【0006】 その為、第2の半導体素子の形状、つまり半導体素子のサイズは、第1の半導体素子上に形成される電極により規制され、上に積層する第2の半導体素子の形状は第1の半導体素子の形状に比べて小さくする必要が生じていた。つまり、従来のMCP構造を有する半導体装置では、略同一形状の半導体素子を複数個実装し、MCP構造を構成する半導体装置を提供することができない

かった。

【0007】 そこで、本発明では、MCP構造を有する半導体装置において、略同一形状を有する複数の半導体素子を実装可能なMCP構造の半導体装置、及びその製造方法を提供することを目的とする。

【0008】

【課題を解決するための手段】 上記課題を解決するため、本発明に係る1つ半導体装置は、第1の面を有する第1の基板、及びその第1の面上に配置される第2の基板とからなる配線基板と、第1の面より前記第1の基板に形成される凹部と、凹部に対応する第2の基板に設けられ、凹部に対応する領域よりも広い領域に形成される開口部と、凹部内に配置されるとともに、配線基板に電気的に接続される第1の電極を有する第1の半導体素子と、第1の半導体素子と略同一形状を有し、少なくとも一部分が開口部内の第1の面上に配置される第2の半導体素子とから構成されるものである。

【0009】 また、本発明に係るもう1つの半導体装置は、表面及び裏面を有する配線基板と、少なくとも表面

20 に形成される配線と、配線基板に形成され、表面から裏面に至る開口部と、第1の電極が形成された第1の面と第1の面に對向する第2の面とを有し、開口部内に配置される第2の面を有する第1の半導体素子と、第1の電極と配線とを接続する第1の導体と、第1の半導体素子と第1の導体とを封止するとともに、第1の半導体素子を配線基板に固着する封止体と、第2の面上に固定されるとともに、第2の面と固定される第3の面、及び第3の面に對向する第4の面と有し、第4の面には、外部との接続を行なう第2の電極が形成され、かつ、第1の半導体素子と略同一形状を有する第2の半導体素子とから構成されるものである。

【0010】 更に、本発明に係る半導体装置の製造方法

は、表面及び裏面を有する配線基板の第1領域に、表面から裏面に至る開口部を形成する工程と、第1領域よりも小さい面積を有する面と、表面及び裏面間の距離により規定される高さよりも低い高さとからなる凸部を有する実装部材を準備する工程と、裏面より実装部材を挿入し、開口部内に前記凸部を収納する工程と、第1の電極が形成される第1の面と、第1の面に對向する第2の面とを有する第1の半導体素子を開口部内の凸部上に固定する工程と、第1の半導体素子を固定する工程後、第1の電極と前記表面上の配線とを第1の導体で接続する工程と、第1の半導体素子及び第1の導体を封止体で封止するとともに、封止体により第1の半導体素子を配線基板に固着する工程と、固着する工程後、実装部材を除去する工程と、除去する工程後、第2の電極が形成される第3の面とその第3の面に對向する第4の面と有するとともに、第1の半導体素子と略同一形状を有する第2の半導体素子の第4の面を第2の面上に固定する工程とからなるものである。

## 【0011】

【発明の実施の形態】以下、本発明の第1の実施形態について図面を参照して説明する。図1は、本発明の第1の実施形態を示す図であり、MCP構造を有する半導体装置の断面図である。

【0012】図1に示すように、第1の実施形態における半導体装置では、配線3aが設けられた第1の面及びその裏面を有する第1の基板1aと、第1の基板1a上に配置され、その表面に設けられた配線3bを有する第2の基板1bとからなる配線基板2上に、略同一形状を有する複数の半導体素子6a, 6bが実装されている。

【0013】本発明において、略同一形状を有する半導体素子とは、同一種類、又は、異なる機能を有する半導体素子であっても同一のサイズを有する半導体素子のことである。また、各半導体素子を製造する際に生じるサイズのバラツキは考慮せず、実質的に同一形状であるとみなす。具体的には、メモリ、又は、ロジック回路等を構成する半導体素子である。

【0014】本実施形態では、第1の基板1aに、第1の半導体素子6aを搭載する凹部4が設けられており、その凹部4内に、電極8aが上となるよう、第1の半導体素子6aが配置される。この第1の半導体素子6aはエポキシ樹脂等からなる接着材7により固定される。また、第1の基板1aに形成された凹部4に対応する領域よりも広い、第2の基板1bの領域には開口部5が設けられ、その開口部5内に第1の半導体装置6aと略同一形状を有する第2の半導体素子6bが配置されている。この第2の半導体素子6bは第1の面上に設けられた接着材7により多層配線基板2に固定される。

【0015】多層配線基板2に固定された各半導体素子は、第1の半導体素子6a上の電極8a、及び第2の半導体素子6b上の電極8bと、多層配線基板上の配線3a, 3bとが、各々金属細線9等の導体により電気的に接続される。最終的に、各半導体素子と金属細線は、エポキシ樹脂等からなる封止体10で封止される。この際、封止体10は金属細線9を確実に封止する必要があり、封止体10は金属細線9の頂点部分よりも50μm程度上方に設けられていることが望ましい。

【0016】ここで、第1の半導体素子6a上に実装される第2の半導体素子6bは、第1の半導体素子6a上に形成された電極8aを除く位置に配置されている。つまり、電極8aは、第2の半導体素子6bにより規定される領域以外の第1の半導体素子6aの領域に設けられている。これにより、本実施形態における半導体装置では、各半導体素子と多層配線間の電気接続を、一括して行なうことが可能となっている。

【0017】また、本実施形態では、凹部4内に収納される第1の半導体素子6aの電極8aは、第2の半導体素子6bが上方に存在しない辺側にのみ配置され、第1の半導体素子6a上に実装される第2の半導体素子6b

の電極8bは、電極8aが形成された辺と対向する辺側に配置される。このような位置に各電極を配置することで、第1の半導体素子6aと多層配線基板2とを接続する金属細線、及び第2の半導体素子6bと多層配線基板2とを接続する金属細線とが接触する恐れを低減することが可能となる。

【0018】また、本実施形態における半導体装置では、外部との接続が必要となる場合、多層配線基板の表面に形成された配線上に外部接続端子となるバンプ等を設けることで適宜対応することが可能である。

【0019】本実施形態の半導体装置で使用される多層配線基板2は、例えば、ガラスエポキシ樹脂等から形成されている。また、多層配線基板2と各半導体素子を接着する接着材7には、絶縁性のエポキシ系接着剤や接着テープが用いられる。

【0020】以上に述べたように本実施形態によれば、凹部4を有する第1の基板1aと、その凹部よりも広い領域を有する開口部5が形成された第2の基板1bとからなる多層配線基板2を用い、開口部5内の第1の基板が有する第1の面上に設けられた接着材7によって、第1の半導体素子6aとは位置をずらして第2の半導体素子6bが実装されるため、同一形状を有する2つの半導体素子を実装したMCP構造を提供することが可能となる。

【0021】また、第1の面に設けた接着材7により第2の半導体素子6bを固定する場合、第1の半導体素子6aの回路形成面に接触せずに第2の半導体素子6bを多層配線基板2に固定することができる。結果、第1の半導体素子の回路形成面を損傷することなく、高い信頼性を有する半導体装置を提供することができる。

【0022】さらに、本実施形態の半導体装置では、上方に配置される第2の半導体素子6bにより規定される領域と重ならない第1の半導体素子の領域の一辺に、第1の電極8a、そして、第1の電極8aが配置された辺と対向する第2の半導体素子の辺側に第2の電極8bが、各々設けられている。このように各半導体装置の電極を配置することで、各半導体素子と多層配線基板とを接続する金属細線が接触することを防ぐことが可能となる。

【0023】本実施形態では、配線基板として、第1の基板1aの両面、及び第2の基板1bの一つの面に配線3a, 3bが形成された多層配線基板2を例に挙げて説明を行なった。しかし、必ずしも多層に配線が形成された多層配線基板である必要はなく、単層の配線を有した配線基板であってもよい。更に、多層配線基板を使用した場合においては、第1若しくは第2の基板に設けられるスルーホールによって、各配線同士が相互に接続されてもよい。また、本実施形態における配線基板は、必ずしも2つの基板からなる配線基板である必要はなく、例えば、第1の基板1a、第2の基板1bが一体的

に形成されたものであってもよい。

【0024】本第1の実施形態における半導体装置では、開口部5内の第1の基板1a上にのみ接着材7を設け、第2の半導体素子6bを多層配線基板2に固定している。このような構造を有する場合、第1の半導体素子6aの回路形成面の損傷を防ぐ為に、接着材は第1の半導体素子6a上に広がることを防止したほうがよい。その為、第1の基板上に設けられる接着材7は接着材の広がりを抑える必要がある。その結果、第2の半導体素子を固定する接着材としては、ある程度の粘度を有する接着剤、若しくは接着テープ等が用いられることが望ましい。

【0025】しかし、第1の基板上の接着材7のみで十分な接着強度が得られない場合は、第1の半導体素子6a上にも接着材を設けて、第2の半導体素子の固定を行なうことも可能である。但し、このような場合は、第1の半導体素子6aの回路形成面に直接、接着材が設けられることとなる為、接着材を設ける際には第1の半導体素子の回路形成面を損傷しないよう留意する必要がある。

【0026】次に、本発明の第2の実施形態について図面を参照して説明する。図2は、本発明の第2の実施形態を示す図であり、MCP構造を有する半導体装置の断面図である。なお、図2において、第1の実施形態と同一物には同じ符号が用いられている。

【0027】図2に示すように、第2の実施形態における半導体装置では、表面に形成された配線23、及び、裏面に形成された端子12とを有する配線基板22の所定の領域に設けられる開口部11内に、略同一形状を有し、それぞれの半導体素子の裏面同士、つまり、各半導体素子の電極が形成されていない面同士を貼り合わせた第1、及び第2の半導体素子6a、6bが実装されている。本実施形態において、第1、及び第2の半導体素子6a、6bは、例えば、メモリ、又はロジック回路等を構成する半導体素子であり、互いに絶縁性エポキシ系接着剤などからなる接着材7により貼り合わされている。

【0028】また、開口部11内に実装された第1の半導体素子6aの電極8aと配線23とは、金属細線9等の導体により接続され、第1の半導体素子6aと配線基板22とは電気的に接続されている。加えて、第1の半導体素子6aと金属細線9は、エポキシ樹脂からなる封止体10により封止され、この封止体10が第1の半導体素子6aの側面と配線基板22の開口部11の内壁面との間に入りこむことにより、第1の半導体素子6aは配線基板22に固着されている。

【0029】更に、第1の半導体素子6aの裏面に接着される第2の半導体素子6bは、第1の半導体素子に接着される裏面に対向する表面に電極8bを有しており、電極8b以外の第2の半導体素子の表面には、エポキシ樹脂などが塗布されることで、第2の半導体素子の表面

が保護されている。

【0030】ここで、この第2の半導体素子に形成される電極8bは、例えば半田バンプからなる外部接続端子である。この電極8bと配線基板の裏面に設けられる端子12とによって、本実施形態における半導体装置は外部装置に実装される。

【0031】このように、第2の実施形態における半導体装置では、配線基板の裏面に形成された端子12と第2の半導体素子の表面に形成された電極8bとにより外部装置との接続が行われる。その結果、外部装置との良好な電気的接続を維持する必要が生じる場合、配線基板の裏面に形成される端子12と第2の半導体素子の表面に形成される電極8bは、略同一面上に形成されることが望ましい。この場合、第2の半導体素子6bは、その第2の半導体素子の表面と配線基板の裏面とが略同一面を形成する開口部11内の位置に配置されることが望ましい。

【0032】また、本実施形態における配線基板22としては、ガラスエポキシ樹脂からなる基板が用いられており、表面に形成された配線23と裏面に形成された端子12は、基板に設けられたスルーホールにより電気的に接続されている。

【0033】第2の実施形態における半導体装置では、裏面に端子12のみが形成された配線基板22を用いた場合を例に挙げて説明を行なったが、裏面に設けられるものは端子のみに限られるものではなく、表面と同様に配線が形成されていてもよい。但し、このような配線基板の裏面にも配線が形成されている半導体装置においても、外部装置との接続を行なう必要がある場合、半田バンプ等の外部接続端子が裏面の配線上に設けられることにより適宜対応できる。

【0034】以上のように、第2の実施形態における半導体装置によれば、第1の半導体素子6aと第2の半導体素子6bの裏面同士、つまり、それぞれの半導体素子の電極8a、8bが形成されていない面同士を貼り合わせ、配線基板22に設けられた開口部11内に2つの半導体素子を実装する為、回路が形成された第1の半導体素子の表面上にMCP構造を構成する第2の半導体素子が直接積層されることがない。結果、第2の半導体素子の形状が第1の半導体素子の電極により規制されることなく、略同一形状の2つの半導体素子を実装したMCP構造を有する半導体装置を提供することが可能となる。更に、各半導体素子の裏面同士を貼り合わせて配線基板への実装を行なう為、第1の半導体素子の回路形成面の損傷を防ぐことが可能となる。

【0035】加えて、本実施形態における半導体装置では、配線基板22に開口部11を設け、その開口部11内に略同一形状を有する2つの半導体素子6a、6bを実装するようにしたので、配線基板上に各半導体素子を実装する従来のMCP構造の半導体装置に比べ、より薄型

化したMCP構造を有する半導体装置を提供することが可能となる。

【0036】次に、第3の実施形態として、本発明の半導体装置の製造方法の一例を図面を参照して説明する。図3は、本実施形態における半導体装置の製造方法において用いられる実装部材15を示す図であり、図3(a)は上部からの平面図、図3(b)は図3(a)の線分B-Bからの断面図である。また、図4(a)～(e)は、本発明の半導体装置の製造工程を示す図であり、各工程におけるMCP構造の半導体装置を断面から見た図である。なお、図3及び図4においても、第1及び第2の実施形態と同一物には同じ符号が用いられている。

【0037】まず、図3を用いて、本実施形態における半導体装置の製造方法で用いられる実装部材の説明を行なう。

【0038】図3(a)に示すように、本実施形態の製造方法で使用される実装部材15は、粘着性を有するテープよりなる粘着テープ17と、半導体素子が配置される面に粘着性物質が設けられた凸部16とから構成されており、粘着テープ17上に凸部16が搭載された構造となっている。

【0039】ここで、実装部材15を構成する凸部16は、例えば、粘着性を有するテープ、又は、熱硬化性の樹脂により形成される部材の上面に粘着テープ17にも用いられる粘着性を有するテープが接着されたもの等により形成される。

【0040】また、この凸部16の形状は、第1の半導体素子の実装を行なう際、凸部16の全体が配線基板に形成された開口部に収納される必要が生じる為、凸部16は、半導体素子を配置する、配線基板に設けられた開口部の面積よりも小さい面積を有する面と、配線基板の板厚よりも薄い、つまり、配線基板の表面及び裏面間の距離により規定される高さよりも低い高さhにより規定される。

【0041】この凸部の高さhは、配線基板の厚さ、及び開口部に実装される各半導体素子の厚さによって適宜決定され、更に、半導体素子を配置する凸部上の面の面積は、配線基板に設けられる開口部の面積によって決定される。

【0042】ここで、半導体素子を配置する凸部16上の面は、配線基板に設けられる開口部の面積よりも小さい面積を有していれば十分であるが、半導体素子を接着する樹脂からなる封止体の半導体素子裏面への回り込みを防止する為に、開口部の面積とほぼ同一の形状であることが望ましい。

【0043】また、本実施形態において、実装部材15を構成する粘着テープ17には、テープを除去する際に粘着性物質が残らない粘着テープ17、例えばUVテープ、若しくは熱気泡性テープ等が用いられている。これ

らの粘着テープは、紫外線照射及び加熱により、接着力を低下させることが可能である。このような性質を有するテープを粘着テープ17として用いることで、半導体素子の実装を行なう際に実装部材が確実に配線基板に固定されるとともに、半導体素子の実装が終了した後では、裏面の配線等を損傷することなく、実装部材を除去することが可能となる。

【0044】次に、図4を用いて、本発明における半導体装置の製造方法について、詳細に説明する。

【0045】図4(a)に示すように、表面及び裏面に配線43a、43bが形成された配線基板42に、表面から裏面に至る開口部11が設けられる。そして、開口部11内には、図3にて説明した実装部材15の凸部が配線基板の裏面より挿入される。この際、実装部材の粘着シート17は、配線基板42の裏面に接着されている。

【0046】次に、図4(b)に示すように、開口部11内に収納された実装部材15の凸部上に、表面に電極8aを有する第1の半導体素子6aを配置し、開口部11内に第1の半導体素子6aを収納する。この際、電極8aが形成された面が上になるように第1の半導体素子6aを配置する。このとき、第1の半導体素子6aは、凸部上に設けられた粘着性物質により、実装部材15に固定される。

【0047】さらに、半導体素子を開口部11に収納した後、公知のワイヤボンド法を用いて、第1の半導体素子の電極8aと配線基板42の表面に形成された配線43aとを、第1の導体である金属細線9aにて接続し、第1の半導体素子6aと配線基板42とを電気的に接続する。そして、その後、第1の半導体素子6a及び金属細線9aとを、例えばエポキシ樹脂からなる封止体10aにより封止する。このとき、第1の半導体素子6aの側面と配線基板42の開口部11の内壁面との間にも封止体10aが入り込み、この封止体10aによって第1の半導体素子6aは配線基板42に接着される。

【0048】次に、図4(c)に示すように、第1の半導体素子6aを配線基板42に接着した後、第1の半導体素子6a下の実装部材15を除去する。

【0049】実装部材15を除去した後、図4(d)に示すように、先程、配線基板42に実装された第1の半導体素子の開口部11内にある面、つまり、第1の半導体素子の裏面上に、第1の半導体素子の裏面に設けられた接着材7にて、第1の半導体素子6aと略同一形状を有する第2の半導体素子6bの裏面が固定される。ここで、第2の半導体素子の裏面は、第2の半導体素子の電極8bが形成されている面と対向する面のことである。また、第1の半導体素子の裏面上に設けられる接着材7としては、例えばエポキシ樹脂等からなる接着剤が用いられている。

【0050】その後、図4(e)に示すように、先の第

1の半導体素子6 aを実装した場合と同様に、公知のワイヤボンド法により、第2の半導体素子の電極8 bと配線基板4 2の裏面に形成された配線4 3 bとが、第2の導体である金属細線9 bにて接続される。そして、第2の半導体素子6 bと配線基板4 2とが金属細線9 bにより電気的に接続された後、第2の半導体素子6 b及び金属細線9 bは、例えば、エポキシ樹脂等からなる封止部10 bにより封止される。この封止により第2の半導体素子6 bは配線基板4 2に固着される。

【0051】このような工程により、本発明のMCP構造を有する半導体装置は製造される。

【0052】以上に説明したように、本実施形態における製造方法によれば、第1の半導体素子6 aと第2の半導体素子6 bの裏面同士、つまり、それぞれの半導体素子の電極8 a、8 bが形成されていない面同士を貼り合わせ、配線基板4 2に設けられた開口部1 1内に2つの半導体素子を実装することが可能となる為、略同一形状を有する複数の半導体素子を配線基板に実装することが可能となる。

【0053】また、配線基板4 2に開口部1 1を設け、その開口部1 1内に複数の半導体素子6 a、6 bを実装するので、凹部を設けた配線基板上に複数の半導体素子を実装する従来の半導体装置に比べて、更に薄型化したMCP構造の半導体装置を提供することができる。

【0054】加えて、開口部を有した配線基板を使用する本実施形態では、金型等の打ち抜きによる一括した配線基板の加工が可能となる為、ドリル等を用いた研削により加工される凹部を有する配線基板を使用する従来に比べ、配線基板の加工にかかるコストを低く抑えることが可能となる。

【0055】更に、本実施形態における製造方法によれば、開口部に挿入された実装部材の凸部上に第1の半導体素子を配置し、実装を行なうので、実装部材の凸部の高さを調節することで、開口部内の半導体素子の位置を適宜決定することが可能となる。また、実装部材の凸部の高さを調節し、第1の半導体素子を開口部内の所定の位置に実装すれば、配線基板の中心部からの厚さを均等にすることでき、配線基板の反りを防ぐことも可能となる。

【0056】また、本実施形態では、実装部材を用いて第1の半導体素子の実装を行ない、その後、第1の半導体素子の裏面上に第2の半導体素子を配置し、第2の半導体素子の実装を行う。その為、各半導体素子の回路や電極が形成された面に触れることなく、複数の半導体素子が積層されたMCP構造の半導体装置を製造すること可能である。結果、各半導体素子の表面に形成された回路や電極等の損傷を防ぐことができ、より信頼性の高いMCP構造の半導体装置を提供することが可能となる。

【0057】更に、本実施形態における半導体装置の製造方法によれば、それぞれの半導体素子を実装する際

に、各半導体素子の電極と配線基板上の配線との電気的接続が行われる為、各半導体素子に接続された金属細線が重なる心配がない。

【0058】図4に示されるように、本実施形態における製造方法では、第1の半導体素子の電極8 aと配線基板の表面の配線3 a、そして、第2の半導体素子の電極8 bと配線基板の裏面の配線3 bとが金属細線9 a、9 bにより、それぞれ電気的に接続されるMCP構造の半導体装置が提供される。しかし、本実施形態における製造方法では、このような構造の半導体装置にのみ係るものではなく、先の第2の実施形態で詳細に説明したような、外部接続端子となる電極を有する第2の半導体素子を開口部内に実装した半導体装置に適用することも可能である。この場合、図4 (d) に示す工程において、表面に外部接続端子を有する第2の半導体素子を第1の半導体素子の裏面上に配置し、第1の半導体素子の裏面上に設けられた接着材により、第2の半導体素子を固定すればよい。

【0059】

【発明の効果】以上に説明した通り、本発明による半導体装置によれば、回路及び電極が形成された第1の半導体素子の表面上には、第2の半導体素子が直接積層されることのないMCP構造を提供することが可能となる。

【0060】結果、本発明における半導体装置では、第2の半導体素子の形状が第1の半導体素子の電極の位置に規制されることがなくなり、略同一形状を有する2つの半導体素子を配線基板に実装することが可能となる。また、第1の半導体素子の回路及び電極形成面に接触することなく、第2の半導体素子が実装されるので、回路や電極の損傷を防ぐことが可能となり、より信頼性の高いMCP構造の半導体装置を提供することが可能となる。

【0061】加えて、本発明による半導体装置の製造方法によれば、各半導体素子の回路及び電極が形成された面に触れることなく、第1の半導体素子と第2の半導体素子の裏面同士、つまり、それぞれの半導体素子の電極が形成されていない面同士を貼り合わせることが可能となる。この為、先に実装される半導体素子の電極の位置に規制されることはなく、配線基板に設けられた開口部1 1内に略同一形状を有する第2の半導体素子を実装することが可能となる。結果、同一形状を有する2つの半導体素子が実装されたMCP構造を有する半導体装置を提供することができる。

【0062】また、本発明による半導体装置の製造方法によれば、配線基板に開口部を設け、その開口部内に複数の半導体素子を実装することが可能となるので、凹部を設けた配線基板上に複数の半導体素子を実装する従来の半導体装置に比べて、更に薄型化した半導体装置を提供することができる。

50 【図面の簡単な説明】

【図1】第1の実施形態を示す半導体装置の断面図である。

【図2】第2の実施形態を示す半導体装置の断面図である。

【図3】図3の実施形態において用いられる実装部材の平面図、及びB-B断面からの断面図である。

【図4】第3の実施形態における半導体装置の製造方法の各工程を示す断面図である。

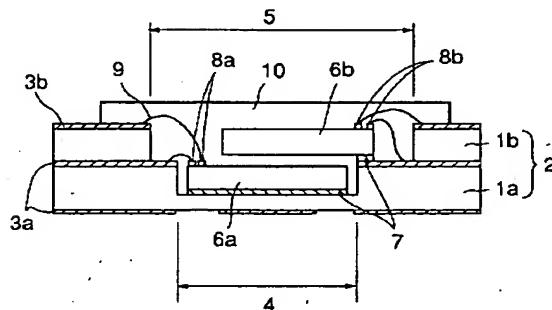
【符号の説明】

2 2 配線基板

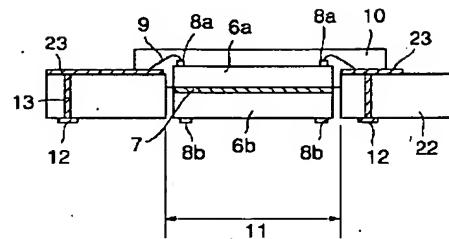
2 3	配線
6 a, 6 b	半導体素子
7	接着材
8 a, 8 b	電極
9	金属細線
1 0	封止体
1 1	開口部
1 2	端子
1 3	スルーホール

10

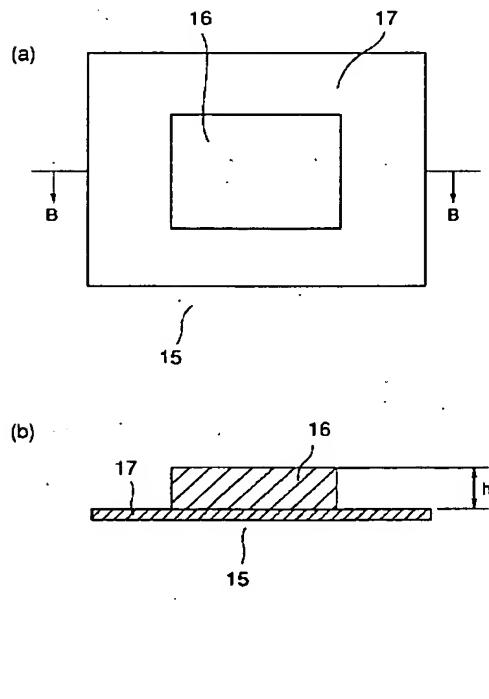
【図1】



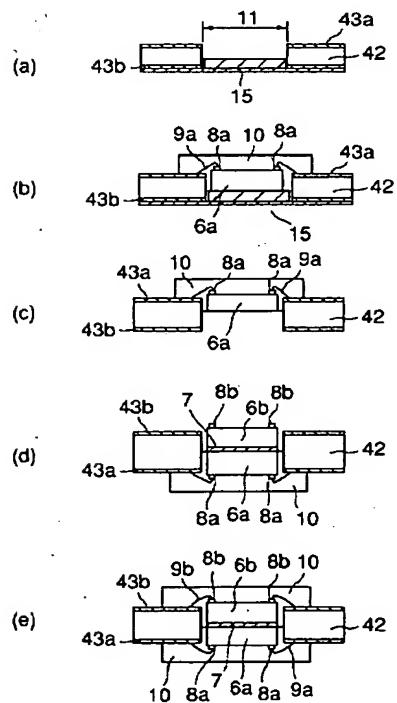
【図2】



【図3】



【図4】



[Claim(s)]

[Claim 1] The 1st substrate which has the 1st field, and the wiring substrate which consists of the 2nd substrate arranged on said 1st field, While being arranged in the crevice formed in said 1st substrate from said 1st field, opening which is prepared in said 2nd substrate corresponding to said crevice, and is formed in a field larger than the field corresponding to said crevice, and said crevice The semiconductor device characterized by having the 1st semiconductor device which has the 1st electrode electrically connected to the circuit pattern formed in said wiring substrate, and the 2nd semiconductor device by which a part is arranged on the 1st [ of said opening circles / said ] field.

[Claim 2] Said 2nd semiconductor device is a semiconductor device according to claim 1 characterized by having said 1st semiconductor device and an abbreviation same configuration.

[Claim 3] Said wiring substrate is a semiconductor device according to claim 1 characterized by forming said the 1st substrate and said 2nd substrate in one.

[Claim 4] It is the semiconductor device which the semiconductor device according to claim 1 has further the metal thin line which connects said the 1st electrode and said wiring substrate electrically, and is characterized by preparing said 1st electrode in the field of said 1st semiconductor device other than the field specified by said 2nd semiconductor device.

[Claim 5] While countering the wiring substrate which has a front face and a rear face, wiring formed in said front face at least, opening from said front face to [ are formed in said wiring substrate and ] said rear face, the 1st field in which the 1st electrode was formed, and said 1st field While closing the 1st conductor which connects the 1st semiconductor device which has said 2nd field arranged at said opening circles, and said 1st electrode and said wiring, and said the 1st semiconductor device and said 1st conductor While being fixed on the closure object which fixes said 1st semiconductor device to said wiring substrate, and said 2nd field The semiconductor device characterized by having said 2nd field, the 3rd field fixed, and the 4th field which counters said 3rd field, and forming in said 4th field the 2nd electrode which makes connection with the exterior, and having said 1st semiconductor device and the 2nd semiconductor device which has an abbreviation same configuration.

[Claim 6] Said rear face and said 4th field are a semiconductor device according to claim 5 characterized by forming the abbreviation same side.

[Claim 7] The process which forms opening from said front face to said rear face in the 1st field of the wiring substrate which has a front face and a rear face, The process for which the

mounting member which has the heights which consist of height lower than the height specified with the distance between the top face which has an area smaller than said 1st field, and said front face and said rear face is prepared, The process which inserts said heights of said mounting member from said rear face, and the 1st field in which the 1st electrode is formed, The process which fixes the 1st semiconductor device which has the 2nd field which counters said 1st field on said heights of said opening circles, While closing the process which connects said 1st electrode and wiring on said front face with the 1st conductor after the process which fixes said 1st semiconductor device, and said the 1st semiconductor device and said 1st conductor with a closure object The process which fixes said 1st semiconductor device to said wiring substrate with said closure object, While having the 3rd field in which the 2nd electrode is formed after the process which removes said mounting member after said process which fixes, and said process to remove, and the 4th field which counters said 3rd field The manufacture approach of the semiconductor device characterized by having the process which fixes said 4th field of said 1st semiconductor device and the 2nd semiconductor device which has an abbreviation same configuration on said 2nd field.

[Claim 8] The manufacture approach of the semiconductor device according to claim 7 characterized by preparing the matter which has adhesiveness on said heights.

[Claim 9] It is the manufacture approach of the semiconductor device according to claim 7 which said mounting member consists of sheets which carry said heights and said heights, and is characterized by said sheet having adhesiveness.

[Claim 10] It is the manufacture approach of the semiconductor device characterized by being the electrode with which said 2nd electrode makes connection with the exterior in the manufacture approach of a semiconductor device according to claim 7.

[Claim 11] The process which fixes said 2nd semiconductor device in the manufacture approach of a semiconductor device according to claim 10 is the manufacture approach of the semiconductor device characterized by being carried out so that said rear face and said 3rd field may form an abbreviation same flat surface.

[Claim 12] The process which connects said 2nd electrode and wiring on said rear face with the 2nd conductor further in the manufacture approach of a semiconductor device according to claim 7 after the process which fixes said 2nd semiconductor device, The manufacture approach of the semiconductor device characterized by having the process which fixes said 2nd semiconductor device to said wiring substrate with the closure object which closes said the 2nd semiconductor device and said 2nd conductor while closing said the 2nd semiconductor device and said 2nd conductor with a closure object.

[Claim 13] While being arranged at the insulating substrate which has the 1st field, the 1st

slot formed in said 1st field, the 2nd slot which is formed in the base of said 1st slot and has an area smaller than the area of said base, and said 2nd Mizouchi The semiconductor device characterized by having the 1st semiconductor device which has the 1st electrode electrically connected to the circuit pattern formed in said insulating substrate, and the 2nd semiconductor device arranged on the 1st [ said ] field which has a part to said 2nd Mizouchi. [Claim 14] Said 2nd semiconductor device is a semiconductor device according to claim 13 characterized by having said 1st semiconductor device and an abbreviation same configuration.

[Claim 15] It is the semiconductor device which the semiconductor device according to claim 13 has further the metal thin line which connects said the 1st electrode and said wiring substrate electrically, and is characterized by preparing said 1st electrode in the field of said 1st semiconductor device other than the field specified by said 2nd semiconductor device.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device in which thin-shape-izing and high density assembly are possible, and its manufacture approach especially about a semiconductor device and its manufacture approach.

[0002]

[Description of the Prior Art] In order to realize conventionally the semiconductor device in which high density assembly is possible, the MCP (Multi-Chip-Package) structure of mounting two or more semiconductor devices in one package is adopted.

[0003] In the semiconductor device which has the usual MCP structure, the 1st semiconductor device which has an electrode on a front face is mounted on the wiring substrate with which circuit wiring was formed. Furthermore, the binder which has insulation is formed on the front face except the electrode of the 1st semiconductor device, and the laminating of the 2nd semiconductor device is carried out by the binder.

[0004] Moreover, in the conventional semiconductor device, after the laminating of the 2nd semiconductor device is carried out on the 1st semiconductor device, the electrode formed in each semiconductor device and circuit wiring formed in the wiring substrate are connected by the metal thin line, and each semiconductor device and a wiring substrate are connected electrically. Furthermore, the closure of each semiconductor device and the metal thin line is carried out with the closure object which consists of resin, and they are protected.

[0005]

[Problem(s) to be Solved by the Invention] However, the semiconductor device which has the conventional MCP structure described above is performing electrical installation of the

1st semiconductor device and a wiring substrate by connecting the electrode which the 2nd semiconductor device is arranged directly and formed on the 1st semiconductor device on the field of the 1st semiconductor device in which the electrode is formed, and circuit wiring on a wiring substrate with a metal thin line.

[0006] For the reason, the configuration of the 2nd semiconductor device, i.e., the size of a semiconductor device, was regulated with the electrode formed on the 1st semiconductor device, and the configuration of the 2nd semiconductor device which turns a laminating up needed to be made small compared with the configuration of the 1st semiconductor device. That is, in the semiconductor device which has the conventional MCP structure, two or more semiconductor devices of an abbreviation same configuration were not able to be mounted, and the semiconductor device which constitutes MCP structure was not able to be offered.

[0007] So, in this invention, it aims at offering the semiconductor device and its manufacture approach of the MCP structure where two or more semiconductor devices which have an abbreviation same configuration can be mounted in the semiconductor device which has MCP structure.

[0008]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, one semiconductor device concerning this invention The 1st substrate which has the 1st field, and the wiring substrate which consists of the 2nd substrate arranged on the 1st field, While being arranged in the crevice formed in said 1st substrate from the 1st field, opening which is prepared in the 2nd substrate corresponding to a crevice, and is formed in a field larger than the field corresponding to a crevice, and a crevice It consists of the 1st semiconductor device which has the 1st electrode electrically connected to a wiring substrate, and the 2nd semiconductor device which has the 1st semiconductor device and abbreviation same configuration and by which at least a part is arranged on the 1st [ of opening circles ] field.

[0009] Moreover, another semiconductor device concerning this invention The wiring substrate which has a front face and a rear face, and wiring formed in a front face at least, The 1st semiconductor device which is formed in a wiring substrate, has opening from a front face to a rear face, and the 1st field in which the 1st electrode was formed and the 2nd field which counters the 1st field, and has the 2nd field arranged at opening circles, While closing the 1st conductor which connects the 1st electrode and wiring, and the 1st semiconductor device and 1st conductor While being fixed on the closure object which fixes the 1st semiconductor device to a wiring substrate, and the 2nd field, it has the 2nd field, the 3rd field fixed, and the 4th field which counters the 3rd field. In the 4th field The 2nd electrode which makes connection with the exterior is formed, and it consists of the 1st

semiconductor device and the 2nd semiconductor device which has an abbreviation same configuration.

[0010] Furthermore, the manufacture approach of the semiconductor device concerning this invention The process which forms opening from a front face to a rear face in the 1st field of the wiring substrate which has a front face and a rear face, The process for which the mounting member which has the heights which consist of height lower than the height specified with the distance between the field which has an area smaller than the 1st field, and a front face and a rear face is prepared, The process which inserts a mounting member and contains said heights from a rear face to opening circles, The process which fixes the 1st semiconductor device which has the 1st field in which the 1st electrode is formed, and the 2nd field which counters the 1st field on the heights of opening circles, While closing the process which connects the 1st electrode and wiring on said front face with the 1st conductor after the process which fixes the 1st semiconductor device, and the 1st semiconductor device and 1st conductor with a closure object While having the process which fixes the 1st semiconductor device to a wiring substrate with a closure object, the process which removes a mounting member after the process which fixes, the 3rd field in which the 2nd electrode is formed after the process to remove, and the 4th field which counters the 3rd field It consists of a process which fixes the 4th field of the 1st semiconductor device and the 2nd semiconductor device which has an abbreviation same configuration on the 2nd field.

[0011]

[Embodiment of the Invention] Hereafter, the 1st operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is drawing showing the 1st operation gestalt of this invention; and is the sectional view of the semiconductor device which has MCP structure.

[0012] As shown in drawing 1 , in the semiconductor device in the 1st operation gestalt, it is arranged on 1st substrate 1a which has the 1st field in which wiring 3a was prepared, and its rear face, and 1st substrate 1a, and two or more semiconductor devices 6a and 6b which have an abbreviation same configuration are mounted on the wiring substrate 2 which consists of the 2nd substrate 1b which has wiring 3b prepared in the front face.

[0013] In this invention, even if the semiconductor device which has an abbreviation same configuration is the same class or a semiconductor device which has a different function, it is a semiconductor device which has the same size. Moreover, the variation in the size produced in case each semiconductor device is manufactured is not taken into consideration, but it is considered that it is the same configuration substantially. Specifically, it is the semiconductor device which constitutes memory or a logical circuit.

[0014] With this operation gestalt, the crevice 4 in which 1st semiconductor device 6a is carried is established in 1st substrate 1a, and 1st semiconductor device 6a is arranged so that electrode 8a may come a top in the crevice 4. This 1st semiconductor device 6a is fixed by the binder 7 which consists of an epoxy resin etc. Moreover, opening 5 is formed in the field of 2nd substrate 1b larger than the field corresponding to the crevice 4 formed in 1st substrate 1a, and 2nd semiconductor device 6b which has 1st semiconductor device 6a and an abbreviation same configuration in the opening 5 is arranged. This 2nd semiconductor device 6b is fixed to the multilayer-interconnection substrate 2 by the binder 7 formed on the 1st field.

[0015] As for each semiconductor device fixed to the multilayer-interconnection substrate 2, electrode 8a on 1st semiconductor device 6a and electrode 8b on 2nd semiconductor device 6b, and the wiring 3a and 3b on a multilayer-interconnection substrate are respectively connected electrically by the conductor of metal thin line 9 grade. Finally, the closure of each semiconductor device and the metal thin line is carried out with the closure object 10 which consists of an epoxy resin etc. Under the present circumstances, the closure object 10 needs to close the metal thin line 9 certainly, and, as for the closure object 10, it is more desirable than the top-most-vertices part of the metal thin line 9 to prepare about 50 micrometers up.

[0016] Here, 2nd semiconductor device 6b mounted on 1st semiconductor device 6a is arranged in the location except electrode 8a formed on 1st semiconductor device 6a. That is, electrode 8a is prepared in the field of 1st semiconductor device 6a other than the field specified by 2nd semiconductor device 6b. It is possible for this to perform electrical connection between each semiconductor device and a multilayer interconnection collectively in the semiconductor device in this operation gestalt.

[0017] Moreover, with this operation gestalt, electrode 8a of 1st semiconductor device 6a contained in crevice 4 a is arranged only at the side side where 2nd semiconductor device 6b does not exist up, and electrode 8b of 2nd semiconductor device 6b mounted on 1st semiconductor device 6a b is arranged at the side [ in which electrode 8a was formed ], and side side which counters. It becomes possible to reduce a possibility that the metal thin line which connects 1st semiconductor device 6a and the multilayer-interconnection substrate 2, and the metal thin line which connects 2nd semiconductor device 6b and the multilayer-interconnection substrate 2 may contact by arranging each electrode in such a location.

[0018] Moreover, when connection with the exterior is needed in the semiconductor device in this operation gestalt, it is possible to correspond suitably by preparing the bump who becomes an external connection terminal on wiring formed in the front face of a

multilayer-interconnection substrate.

[0019] The multilayer-interconnection substrate 2 used with the semiconductor device of this operation gestalt is formed for example, from the glass epoxy resin etc. Moreover, epoxy insulating system adhesives and adhesive tape are used for the binder 7 on which the multilayer-interconnection substrate 2 and each semiconductor device are pasted up.

[0020] 1st substrate 1a which has a crevice 4 according to this operation gestalt as stated above, Using the multilayer-interconnection substrate 2 which consists of the 2nd substrate 1b in which the opening 5 which has a field larger than the crevice was formed with the binder 7 formed on the 1st field which the 1st substrate in opening 5 has It becomes possible [ 1st semiconductor device 6a ] to offer the MCP structure which mounted two semiconductor devices which have the same configuration, since a location is shifted and 2nd semiconductor device 6b is mounted.

[0021] Moreover, when it fixes 2nd semiconductor device 6b with the binder 7 formed in the 1st field, 2nd semiconductor device 6b can be fixed to the multilayer-interconnection substrate 2, without contacting the circuit forming face of 1st semiconductor device 6a. The semiconductor device which has high dependability can be offered without damaging a result and the circuit forming face of the 1st semiconductor device.

[0022] Furthermore, in the semiconductor device of this operation gestalt, 2nd electrode 8b is respectively prepared in the side [ where the 1st electrode 8a and 1st electrode 8a have been arranged at one side of the field of the 1st semiconductor device which does not lap with the field specified by 2nd semiconductor device 6b arranged up ], and side side of the 2nd semiconductor device which counters. Thus, it becomes possible to prevent the metal thin line which connects each semiconductor device and a multilayer-interconnection substrate contacting by arranging the electrode of each semiconductor device.

[0023] This operation gestalt explained by mentioning as an example the multilayer-interconnection substrate 2 with which Wiring 3a and 3b was formed in both sides of 1st substrate 1a, and one field of 2nd substrate 1b as a wiring substrate. However, it is not necessary to be the multilayer-interconnection substrate with which wiring was not necessarily formed in the multilayer, and you may be a wiring substrate with wiring of a monolayer. Furthermore, each wiring may be mutually connected by the through hole established in the 1st or the 2nd substrate when a multilayer-interconnection substrate is used. Moreover, the wiring substrate in this operation gestalt does not necessarily need to be a wiring substrate which consists of two substrates, for example, the 1st substrate 1a and 2nd substrate 1b may be formed in one.

[0024] In the semiconductor device in the operation gestalt of \*\*\*\* 1, a binder 7 is formed only on 1st [ in opening 5 ] substrate 1a, and 2nd semiconductor device 6b is fixed to the

multilayer-interconnection substrate 2. It is better to prevent that a binder spreads on 1st semiconductor device 6a, in order to prevent damage on the circuit forming face of 1st semiconductor device 6a, when it has such structure. For the reason, the binder 7 formed on the 1st substrate needs to stop the breadth of a binder. Consequently, it is desirable to use the adhesives which have a certain amount of viscosity as a binder which fixes the 2nd semiconductor device, or adhesive tape.

[0025] However, when bond strength sufficient with just the binder 7 on the 1st substrate is not obtained, it is also possible to form a binder also on 1st semiconductor device 6a, and to fix the 2nd semiconductor device. However, in such a case, in case a binder is formed, it is necessary to take care, since a binder will be directly formed in the circuit forming face of 1st semiconductor device 6a so that the circuit forming face of the 1st semiconductor device may not be damaged.

[0026] Next, the 2nd operation gestalt of this invention is explained with reference to a drawing: Drawing 2 is drawing showing the 2nd operation gestalt of this invention, and is the sectional view of the semiconductor device which has MCP structure. In addition, the same sign is used for the same object as the 1st operation gestalt in drawing 2.

[0027] As shown in drawing 2, in the semiconductor device in the 2nd operation gestalt In the opening 11 prepared in the predetermined field of the wiring substrate 22 which has the wiring 23 formed in the front face, and the terminal 12 formed in the rear face It has an abbreviation same configuration and the 1st and 2nd semiconductor devices 6a and 6b which stuck the rear faces of each semiconductor device, i.e., the fields in which the electrode of each semiconductor device is not formed, are mounted. In this operation gestalt, it is the semiconductor device which constitutes memory or a logical circuit, and the 1st and 2nd semiconductor devices 6a and 6b are stuck by the binder 7 which consists of insulating epoxy system adhesives etc. mutually.

[0028] Moreover, electrode 8a and wiring 23 of 1st semiconductor device 6a which were mounted in opening 11 are connected by the conductor of metal thin line 9 grade, and 1st semiconductor device 6a and the wiring substrate 22 are connected electrically. In addition, the closure of 1st semiconductor device 6a and the metal thin line 9 was carried out with the closure object 10 which consists of an epoxy resin, and when this closure object 10 enters between the side face of 1st semiconductor device 6a, and the internal surface of the opening 11 of the wiring substrate 22, they have fixed 1st semiconductor device 6a to the wiring substrate 22.

[0029] Furthermore, 2nd semiconductor device 6b pasted up on the rear face of 1st semiconductor device 6a has electrode 8b on the front face which counters the rear face pasted up on the 1st semiconductor device, it is that an epoxy resin etc. is applied and the

front face of the 2nd semiconductor device is protected by the front face of the 2nd semiconductor device other than electrode 8b.

[0030] Here, electrode 8b formed in this 2nd semiconductor device is an external connection terminal which consists for example, of a solder bump. With this electrode 8b and the terminal 12 prepared in the rear face of a wiring substrate, the semiconductor device in this operation gestalt is mounted in an external device.

[0031] Thus, connection with an external device is made in the semiconductor device in the 2nd operation gestalt by electrode 8b formed in the front face of the terminal 12 formed in the rear face of a wiring substrate, and the 2nd semiconductor device. Consequently, when good electrical installation with an external device will need to be maintained, as for electrode 8b formed in the front face of the terminal 12 formed in the rear face of a wiring substrate, and the 2nd semiconductor device, being formed on an abbreviation same side is desirable. In this case, as for 2nd semiconductor device 6b, it is desirable to be arranged in the location in the opening 11 in which the front face of that 2nd semiconductor device and the rear face of a wiring substrate form an abbreviation same side.

[0032] Moreover, as a wiring substrate 22 in this operation gestalt, the substrate which consists of a glass epoxy resin is used; and the wiring 23 formed in the front face and the terminal 12 formed in the rear face are electrically connected by the through hole established in the substrate.

[0033] Although the semiconductor device in the 2nd operation gestalt explained by mentioning as an example the case where the wiring substrate 22 with which only the terminal 12 was formed in the rear face is used, what is prepared in a rear face is not restricted only to a terminal, and wiring may be formed like the front face. However, also in the semiconductor device with which wiring is formed also in the rear face of such a wiring substrate, when connection with an external device needs to be made, it can respond suitably by preparing external connection terminals, such as a solder bump, on wiring on the back.

[0034] According to the semiconductor device in the 2nd operation gestalt, as mentioned above, the rear faces of 1st semiconductor device 6a and 2nd semiconductor device 6b The fields in which the electrodes 8a and 8b of each semiconductor device are not formed That is, lamination, Since two semiconductor devices are mounted in the opening 11 prepared in the wiring substrate 22, the direct laminating of the 2nd semiconductor device which constitutes MCP structure on the front face of the 1st semiconductor device in which the circuit was formed is not carried out. It becomes possible to offer the semiconductor device which has the MCP structure which mounted two semiconductor devices of an abbreviation same configuration, without regulating the configuration of a result and the 2nd

semiconductor device with the electrode of the 1st semiconductor device. Furthermore, in order to stick the rear faces of each semiconductor device and to perform mounting to a wiring substrate, it becomes possible to prevent damage on the circuit forming face of the 1st semiconductor device.

[0035] In addition, since it was made to mount two semiconductor devices 6a and 6b which form opening 11 in the wiring substrate 22, and have an abbreviation same configuration in the opening 11 in the semiconductor device in this operation gestalt, it becomes possible to offer the semiconductor device which has the MCP structure thin-shape-sized more compared with the semiconductor device of the conventional MCP structure of mounting each semiconductor device on a wiring substrate.

[0036] Next, an example of the manufacture approach of the semiconductor device of this invention is explained with reference to a drawing as 3rd operation gestalt. Drawing 3 is drawing showing the mounting member 15 used in the manufacture approach of the semiconductor device in this operation gestalt, drawing 3 (a) is a top view from the upper part, and drawing 3 (b) is a sectional view from segment B-B of drawing 3 (a). Moreover, drawing 4 (a) - (e) is drawing showing the production process of the semiconductor device of this invention, and is drawing which looked at the semiconductor device of the MCP structure in each process from the cross section. In addition, the same sign is used for the same object as the 1st and 2nd operation gestalten also in drawing 3 and drawing 4.

[0037] First, the mounting member used by the manufacture approach of the semiconductor device in this operation gestalt is explained using drawing 3.

[0038] As shown in drawing 3 (a), the mounting member 15 used by the manufacture approach of this operation gestalt consists of adhesive tape 17 which consists of a tape which has adhesiveness, and heights 16 by which slime was prepared in the field where a semiconductor device is arranged, and has the structure where the adhesive tape 17 convex section 16 was carried.

[0039] Here, the heights 16 which constitute the mounting member 15 are formed of what the tape which has adhesiveness, or the tape which has the adhesiveness used also for adhesive tape 17 on the top face of the member formed with thermosetting resin pasted up.

[0040] Since the whole heights 16 will need to be contained by opening formed in the wiring substrate in case the 1st semiconductor device is mounted, the configuration of these heights 16 moreover, heights 16 It is thinner than the board thickness of a wiring substrate, that is, the field which has an area smaller than the area of opening prepared in the wiring substrate which arranges a semiconductor device is prescribed by height h lower than the height specified with the distance between the front face of a wiring substrate, and a rear face.

[0041] Height  $h$  of these heights is suitably determined by the thickness of a wiring substrate, and the thickness of each semiconductor device mounted in opening, and the area of the field on the heights which arrange a semiconductor device is further determined by the area of opening prepared in a wiring substrate.

[0042] Although the field on the heights 16 which arrange a semiconductor device is enough if it has an area smaller than the area of opening prepared in a wiring substrate, in order to prevent the surroundings lump by the semiconductor device rear face of the closure object which consists of resin which fixes a semiconductor device here, it is desirable that it is the almost same configuration as the area of opening.

[0043] Moreover, in this operation gestalt, in case a tape is removed, the adhesive tape 17 with which slime does not remain, for example, UV tape, a thermal-bubble nature tape, etc. are used for the adhesive tape 17 which constitutes the mounting member 15. These adhesive tape can reduce adhesive strength with UV irradiation and heating. It becomes possible to remove a mounting member, without damaging wiring on the back etc., after mounting of a semiconductor device is completed while a mounting member is certainly fixed to a wiring substrate by using the tape which has such a property as adhesive tape 17, in case a semiconductor device is mounted.

[0044] Next, the manufacture approach of the semiconductor device in this invention is explained to a detail using drawing 4 .

[0045] As shown in drawing 4 (a), the opening 11 from a front face to a rear face is formed in the wiring substrate 42 with which Wiring 43a and 43b was formed in the front face and the rear face. And into opening 11, the heights of the mounting member 15 explained by drawing 3 are inserted from the rear face of a wiring substrate. Under the present circumstances, the pressure sensitive adhesive sheet 17 of a mounting member is pasted up on the rear face of the wiring substrate 42.

[0046] Next, as shown in drawing 4 (b), on the heights of the mounting member 15 contained in opening 11, 1st semiconductor device 6a which has electrode 8a on a front face is arranged, and 1st semiconductor device 6a is contained in opening 11. Under the present circumstances, 1st semiconductor device 6a is arranged so that the field in which electrode 8a was formed may turn up. At this time, 1st semiconductor device 6a is fixed to the mounting member 15 with the slime prepared on heights.

[0047] Furthermore, after containing a semiconductor device to opening 11, electrode 8a of the 1st semiconductor device and wiring 43a formed in the front face of the wiring substrate 42 are connected in metal thin line 9a which is the 1st conductor using the well-known wire bond method, and 1st semiconductor device 6a and the wiring substrate 42 are connected electrically. And the 1st semiconductor device 6a and metal thin line 9a are closed after that

by closure object 10a which consists of an epoxy resin. At this time, the closure object 10 enters also between the side face of 1st semiconductor device 6a, and the internal surface of the opening 11 of the wiring substrate 42, and 1st semiconductor device 6a fixes to the wiring substrate 42 by this closure object 10a.

[0048] Next, as shown in drawing 4 (c), after fixing 1st semiconductor device 6a to the wiring substrate 42, the mounting member 15 under 1st semiconductor device 6a is removed.

[0049] On the field in the opening 11 of the 1st semiconductor device mounted in the wiring substrate 42, i.e., the rear face of the 1st semiconductor device, after removing the mounting member 15, as shown in drawing 4 (d), the rear face of 1st semiconductor device 6a and 2nd semiconductor device 6b which has an abbreviation same configuration is previously fixed with the binder 7 formed in the rear face of the 1st semiconductor device. Here, the rear faces of the 2nd semiconductor device are the field in which electrode 8b of the 2nd semiconductor device is formed, and a field which counters. Moreover, as a binder 7 formed on the rear face of the 1st semiconductor device, the adhesives which consist of an epoxy resin etc., for example are used.

[0050] Then, as shown in drawing 4 (e), electrode 8b of the 2nd semiconductor device and wiring 43b formed in the rear face of the wiring substrate 42 are connected by the well-known wire bond method like the case where 1st previous semiconductor device 6a is mounted, in metal thin line 9b which is the 2nd conductor. And after 2nd semiconductor device 6b and the wiring substrate 42 are electrically connected by metal thin line 9b, the closure of the 2nd semiconductor device 6b and the metal thin line 9b is carried out by closure object 10b which consists of an epoxy resin etc. 2nd semiconductor device 6b fixes to the wiring substrate 42 by this closure.

[0051] According to such a process, the semiconductor device which has the MCP structure of this invention is manufactured.

[0052] As explained above, according to the manufacture approach in this operation gestalt, the rear faces of 1st semiconductor device 6a and 2nd semiconductor device 6b That is, since it becomes possible to mount two semiconductor devices in the opening 11 in which the fields in which the electrodes 8a and 8b of each semiconductor device are not formed were established by lamination and the wiring substrate 42, it becomes possible to mount two or more semiconductor devices which have an abbreviation same configuration in a wiring substrate.

[0053] Moreover, since opening 11 is formed in the wiring substrate 42 and two or more semiconductor devices 6a and 6b are mounted in the opening 11, compared with the conventional semiconductor device which mounts two or more semiconductor devices on the wiring substrate which prepared the crevice, the semiconductor device of the MCP

structure thin-shape-ized further can be offered.

[0054] In addition, since it becomes processible [ the wiring substrate by punching, such as metal mold, put in block ] with this operation gestalt which uses a wiring substrate with opening, it becomes possible to hold down the cost concerning processing of a wiring substrate low compared with the former which uses the wiring substrate which has the crevice processed by the grinding using a drill etc.

[0055] Furthermore, since it mounts by arranging the 1st semiconductor device on the heights of the mounting member inserted in opening according to the manufacture approach in this operation gestalt, it becomes possible to determine the location of the semiconductor device of opening circles suitably by adjusting the height of the heights of a mounting member. Moreover, if the height of the heights of a mounting member is adjusted and the 1st semiconductor device is mounted in the position of opening circles, thickness from the core of a wiring substrate can be equalized and it will also become possible to prevent the curvature of a wiring substrate.

[0056] Moreover, with this operation gestalt, the 1st semiconductor device is mounted using a mounting member, after that, on the rear face of the 1st semiconductor device, the 2nd semiconductor device is arranged and the 2nd semiconductor device is mounted. It is possible to manufacture the semiconductor device of the MCP structure where the laminating of two or more semiconductor devices was carried out, without touching the field in which the circuit and electrode of each semiconductor device were formed for the reason. The damage on a circuit, an electrode, etc. formed in the result and the front face of each semiconductor device can be prevented, and it becomes possible to offer the semiconductor device of more reliable MCP structure.

[0057] Furthermore, since according to the manufacture approach of the semiconductor device in this operation gestalt electrical installation of the electrode of each semiconductor device and wiring on a wiring substrate is performed in case each semiconductor device is mounted, there is no fear of the metal thin line connected to each semiconductor device lapping.

[0058] As shown in drawing 4 , by the manufacture approach in this operation gestalt, the semiconductor device of the MCP structure where electrode 8a of the 1st semiconductor device, wiring 3a of the front face of a wiring substrate, electrode 8b of the 2nd semiconductor device, and wiring 3b of the rear face of a wiring substrate are electrically connected by the metal thin lines 9a and 9b, respectively is offered. However, it is also possible to apply to the semiconductor device which mounted the 2nd semiconductor device which has an electrode used as an external connection terminal which was explained to the detail with the 2nd previous operation gestalt in opening circles instead of the thing only

concerning the semiconductor device of such structure by the manufacture approach in this operation gestalt. In this case, what is necessary is to arrange the 2nd semiconductor device which has an external connection terminal on a front face on the rear face of the 1st semiconductor device, and just to fix the 2nd semiconductor device with the binder formed on the rear face of the 1st semiconductor device in the process shown in drawing 4 (d).

[0059]

[Effect of the Invention] According to the semiconductor device by this invention, on the front face of the 1st semiconductor device in which the circuit and the electrode were formed, it becomes possible to offer the MCP structure where the direct laminating of the 2nd semiconductor device is not carried out as explained above.

[0060] In the semiconductor device in a result and this invention, it is removed that the configuration of the 2nd semiconductor device is regulated by the location of the electrode of the 1st semiconductor device, and it becomes possible to mount two semiconductor devices which have an abbreviation same configuration in a wiring substrate. Moreover, since the 2nd semiconductor device is mounted without contacting the 1st circuit and electrode forming face of a semiconductor device, it becomes possible to prevent damage on a circuit or an electrode, and it becomes possible to offer the semiconductor device of more reliable MCP structure.

[0061] In addition, it becomes possible to stick the rear faces of the 1st semiconductor device and the 2nd semiconductor device, i.e., the fields in which the electrode of each semiconductor device is not formed, without touching the field in which the circuit and electrode of each semiconductor device were formed according to the manufacture approach of the semiconductor device by this invention. For this reason, it becomes possible to mount the 2nd semiconductor device which has an abbreviation same configuration in the opening 11 which is not regulated by the location of the electrode of the semiconductor device mounted previously, and was prepared in the wiring substrate. The semiconductor device which has the MCP structure where a result and two semiconductor devices which have the same configuration were mounted can be offered.

[0062] Moreover, since it becomes possible to prepare opening in a wiring substrate and to mount two or more semiconductor devices in the opening circles according to the manufacture approach of the semiconductor device by this invention, compared with the conventional semiconductor device which mounts two or more semiconductor devices on the wiring substrate which prepared the crevice, the semiconductor device thin-shape-ized further can be offered.

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the semiconductor device in which the 1st operation

gestalt is shown.

[Drawing 2] It is the sectional view of the semiconductor device in which the 2nd operation gestalt is shown.

[Drawing 3] They are the top view of the mounting member used in the operation gestalt of drawing 3, and a sectional view from a B-B cross section.

[Drawing 4] It is the sectional view showing each process of the manufacture approach of the semiconductor device in the 3rd operation gestalt.

[Description of Notations]

22 Wiring Substrate

23 Wiring

6a, 6b Semiconductor device

7 Binder

8a, 8b Electrode

9 Metal Thin Line

10 Closure Object

11 Opening

12 Terminal

13 Through Hole